In the Claims:

Please amend claims 1-20. The claims are as follows:

1. (Currently amended) A delay cell, comprising:

a latch comprising a first circuit and a second circuit being cross-coupled together;

a first transistor circuit~~circuit logic gate~~ and a first circuit capacitor both being electrically coupled to an output of the first circuit such that the first circuit, the first transistor circuit~~circuit logic gate~~, and the first circuit capacitor being in series; and

a first input transistor~~logic gate~~ electrically coupled to ~~an~~ said output of the first circuit, wherein the first input transistor~~logic gate~~ is configured to switch states in response to a voltage level of a gate terminal of the first input transistor, and wherein the first and second circuits are configured to switch states at time t1 in response to the first input transistor~~logic gate~~ switching states at time t2, ~~with~~wherein a delay time between t1 and t2 depends~~depending~~ on ~~the~~ a voltage level of a gate terminal of the first transistor circuit~~circuit logic gate~~.

2. (Currently amended) The delay cell of claim 1, further comprising a second transistor circuit~~circuit~~ logic gate and a second circuit capacitor both electrically coupled to the second circuit such that the second circuit, the second transistor circuit~~circuit logic gate~~, and the second circuit capacitor being in series, wherein the delay time between t1 and t2 further depends on ~~the~~ a voltage level of a gate terminal of the second transistor circuit~~circuit logic gate~~.

3. (Currently amended) The delay cell of claim 2, wherein the gate terminal of the first transistor circuit~~circuit logic gate~~ and the gate terminal of the second transistor circuit~~circuit logic gate~~ are electrically coupled together.

4. (Currently amended) The delay cell of claim 1, further comprising:

a first pull-up transistor circuit~~logic gate~~ electrically coupled between the output of the first circuit and a voltage supply;

a first gate-terminal capacitor; and

a first gate-terminal transistor circuit~~logic gate~~,

wherein the first gate-terminal capacitor and the first gate-terminal transistor circuit~~logic gate~~ are electrically coupled together such that the first gate-terminal capacitor and the first gate-terminal transistor circuit~~logic gate~~ are in series between an input of the first circuit and a gate terminal of the first pull-up transistor circuit~~logic gate~~, and wherein the time delay between t1 and t2 further depends on ~~the~~ a voltage level of a gate terminal of the first gate-terminal transistor circuit~~logic~~ gate.

5. (Currently amended) The delay cell of claim 4, further comprising:

a second pull-up transistor circuit~~logic gate~~ electrically coupled between the input of the first circuit and the voltage supply;

a second gate-terminal capacitor; and

a second gate-terminal transistor circuit~~logic gate~~,

wherein the second gate-terminal capacitor and the second gate-terminal transistor circuit~~logic gate~~ are electrically coupled together such that the second gate-terminal capacitor and the second gate-terminal transistor circuit~~logic gate~~ are in series between the output of the first circuit and a gate terminal of the second pull-up transistor circuit~~logic gate~~, and wherein the time delay between t1 and t2 further depends on ~~the~~ a voltage level of a gate terminal of second gate-terminal transistor circuit~~logic gate~~.

6. (Currently amended) The delay cell of claim 5, wherein the gate terminal of the first gate-terminal transistor circuit~~logic gate~~ and the gate terminal of the second gate-terminal transistor circuit~~logic gate~~ are electrically coupled together.

7. (Currently amended) The delay cell of claim 1, further comprising a second input transistor~~logic gate~~ electrically coupled to an input of the first circuit, wherein the second input transistor~~logic gate~~ is configured to have states opposite to that of the first input transistor~~logic~~ gate.

8. (Currently amended) The delay cell of claim 1, further comprising:

a cross-output transistor circuit~~logic gate~~; and

a cross-output capacitor,

wherein the cross-output transistor circuit~~logic gate~~ and the cross-output capacitor are electrically coupled together such that the cross-output transistor circuit~~logic gate~~ and the cross-output capacitor are in series between the output of the first circuit and an output of the second circuit, and wherein the time delay between t1 and t2 further depends on ~~the~~ a voltage level of a gate terminal of the cross-output transistor circuit~~logic gate~~.

9. (Currently amended) A method for operating a delay cell, the method comprising the steps of:

providing in the delay cell (i) a latch comprising a first circuit and a second circuit being cross coupled together, (ii) a first transistor circuit~~circuit logic gate~~ and a first circuit capacitor both being electrically coupled to an output of the first circuit such that the first circuit, the first transistor circuit~~circuit logic gate~~, and the first circuit capacitor being in series, and (iii) a first input transistor~~logic gate~~ electrically coupled to ~~an~~ said output of the first circuit;

switching states of the first input transistor~~logic gate~~ in response to a voltage level of a gate terminal of the first input transistor; and

switching states of the first and second circuits at time t1 in response to the first input transistor~~logic gate~~ switching states at time t2, ~~with~~wherein a delay time between t1 and t2 dependsdepending on ~~the~~ a voltage level of a gate terminal of the first transistor circuit~~circuit logic gate~~.

10. (Currently amended) The method of claim 9, further comprising the steps of:

providing further in the delay cell a second transistor circuit~~circuit logic gate~~ and a second circuit capacitor both electrically coupled to the second circuit such that the second circuit, the second transistor circuit~~circuit logic gate~~, and the second circuit capacitor being in series; and

switching states of the first and second circuits in response to the first input transistor~~logic~~ gate switching states, with the delay time between t1 and t2 dependsdepending on ~~the~~ a voltage level of a gate terminal of the second transistor circuit~~circuit logic gate~~.

11. (Currently amended) The method of claim 10, wherein the gate terminal of the first transistor circuit~~circuit logic gate~~ and the gate terminal of the second transistor circuit~~circuit logic gate~~ are electrically coupled together.

12. (Currently amended) The method of claim 9, further comprising the steps of:

providing further in the delay cell (i) a first pull-up transistor circuit~~logic gate~~ electrically coupled between the output of the first circuit and the voltage supply, (ii) a first gate-terminal capacitor, and (iii) a first gate-terminal transistor circuit~~logic gate~~, wherein the first gate-terminal capacitor and the first gate-terminal transistor circuit~~logic gate~~ being electrically coupled together such that the first gate-terminal capacitor and the first gate-terminal transistor circuit~~logic gate~~ are in series between an input of the first circuit and a gate terminal of the first pull-up transistor circuit~~logic gate~~; and

switching states of the first and second circuits in response to the first input transistor~~logic gate~~ switching states, with the delay time between t1 and t2 depends~~depending~~ on the a voltage level of a gate terminal of the first gate-terminal transistor circuit~~logic gate~~.

13. (Currently amended) The method of claim 12, further comprising the steps of:

providing further in the delay cell (i) a second pull-up transistor circuit~~logic gate~~ electrically coupled between the input of the first circuit and the voltage supply, (ii) a second gate-terminal capacitor, and (iii) a second gate-terminal transistor circuit~~logic gate~~, wherein the second gate-terminal capacitor and the second gate-terminal transistor circuit~~logic gate~~ being electrically coupled together such that the second gate-terminal capacitor and the second gate-terminal transistor circuit~~logic gate~~ are in series between the output of the first circuit and a gate

terminal of the second pull-up transistor circuit~~logic gate~~; and

switching states of the first and second circuits in response to the first input transistor~~logic gate~~ switching states, with the delay time between t1 and t2 depends~~depending~~ on ~~the~~ a voltage level of a gate terminal of the second gate-terminal transistor circuit~~logic gate~~.

14. (Currently amended) The method of claim 13, wherein the gate terminal of the first gate-terminal transistor circuit~~logic gate~~ and the gate terminal of the second gate-terminal transistor circuit~~logic gate~~ are electrically coupled together.

15. (Currently amended) The method of claim 9, further comprising the steps of:

providing in the delay cell a second input transistor~~logic gate~~ electrically coupled to an input of the first circuit; and

switching states of the second input transistor~~logic gate~~ in response to the first input transistor~~logic gate~~ switching states such that the states of the second input transistor~~logic gate~~ are opposite of that of the first input transistor~~logic gate~~.

16. (Currently amended) The method of claim 9, further comprising the steps of:

providing further in the delay cell (i) a cross-output transistor circuit~~logic gate~~, and (ii) a cross-output capacitor, the cross-output transistor circuit~~logic gate~~ and the cross-output capacitor being electrically coupled together such that the cross-output transistor circuit~~logic gate~~ and the cross-output capacitor are in series between the output of the first circuit and an output of the second circuit; and

switching states of the first and second circuits in response to the first input transistor~~logic gate~~ switching states, with the delay time between t1 and t2 depends~~depending~~ on the~~-~~ a voltage level of a gate terminal of the cross-output transistor circuit~~logic gate~~.

17. (Currently amended) A structure, comprising:

a latch;

an input transistor~~logic gate~~, electrically coupled to a first output of the latch; and

a first impedance circuit electrically coupled to the first output of the latch such that the first impedance circuit and the latch are in series, wherein the first impedance circuit is configured such that a resistance of the first impedance circuit changes ~~to change its resistance~~ in response to a control signal, and wherein the latch is configured to switch states at time t1 in response to the input transistor~~logic gate~~ switching states at time t2, ~~with~~wherein a delay time between t1 and t2 depends~~depending~~ on ~~the~~ a resistance of the first impedance circuit.

18. (Currently amended) The structure of claim 17, wherein the first impedance circuit comprises a latch-coupled capacitor and a latch transistor circuit~~logic gate~~ electrically coupled in series, wherein ~~the~~ a resistance of the latch transistor circuit~~logic gate~~ depends on ~~the~~ a voltage level at a gate terminal of the latch transistor circuit~~logic gate~~.

19. (Currently amended) The structure of claim 17, further comprising:

a pull-up transistor circuit~~logic gate~~ electrically coupled between the first output of the latch and a voltage supply; and

a second impedance circuit electrically coupled between a second output of the latch and a gate terminal of the pull-up transistor circuit~~logic gate~~,

wherein the delay time between t1 and t2 further depends on ~~the~~ a resistance of the second impedance circuit.

20. (Currently amended) The structure of claim 19, wherein the second impedance circuit comprises a gate-terminal capacitor and a gate-terminal transistor circuit~~logic gate~~ electrically coupled in series, and wherein ~~the~~ a resistance of the gate-terminal transistor circuit~~logic~~ gate depends on ~~the~~ a voltage level at a gate terminal of the gate-terminal transistor circuit~~logic gate~~.